Agilent 71612 Error Performance Analyzer

Quick Reference (71612-90017)

This booklet is intended as a handy reminder of the fundamentals of BER measurement and of how to use the Agilent 71612 Error Performance Analyzer for BER measurements.

Full details of all the steps and procedures are given in the 71612 Operating and Programming Manual. We recommend that you read the full manual before using this booklet.

Contents

CAUTION

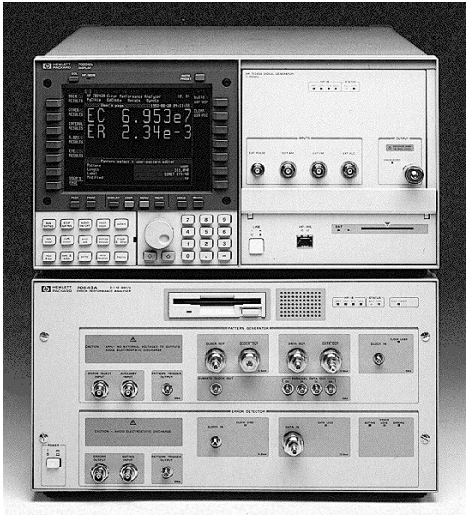
All of the 71612 data and clock outputs are dc-coupled.
DO NOT APPLY ANY EXTERNAL VOLTAGE TO THESE OUTPUTS.
This will damage the internal amplifiers.

Take particular care when using a bias tee to connect it the correct way.

Intro to the 71612

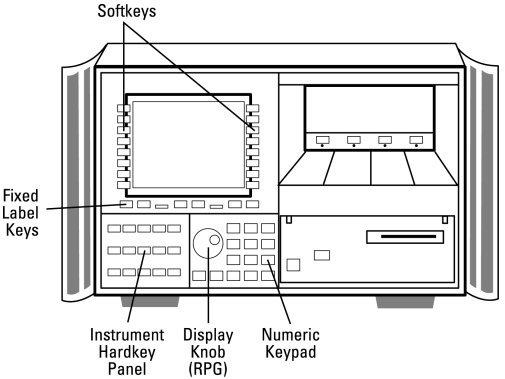
Agilent 71612
12.5 Gb/s Error Performance Analyzer

Intro to the 71612



The Front Panel

The 70004A Display serves as the front panel for instruments in the 71612 Series, and as your window for viewing current system configuration and measurement results.



Instrument Hardkeys

instrument hardkeys gain instant access to primary instrument functions such as ***data output*** or ***result pages***.

The keys are color-coded to indicate their function:

- ***Green*** for configuration keys
- ***Blue*** for result pages
- ***Black*** for immediate selection keys for gating and audio.

Instrument Softkeys

softkeys select instrument functions. The functions are organized in groups, called softkey menus.

NOTE Softkeys that are selected are displayed in inverse video or are underlined.

Some softkeys switch between two states, such as **LOGGING OFF ON** and **SYNC AUTO/MAN**. An underline on the key labels indicates which keys and conditions are selected.

Softkeys and Windows Color Coding

Softkeys and windows are color coded to indicate the primary instrument functions with which they are associated. They are:

- **Blue softkeys/window:** assigned to Results Page occupies two thirds of screen.
- **Green softkeys/window:** assigned to pattern generator/ error detector configuration
- **Yellow softkeys - green/yellow window:** assigned to Pattern Editor
- **Grey softkeys/window:** assigned to user pattern selection and save.
- Softkeys that are “greyed out” are not valid for the currently selected instrument function.

Fixed Label Keys

FIXED LABEL keys select major system functions such as PRINT, PLOT, INSTR PRESET, DISPLAY or MENU.

Access display functions by pressing DISPLAY. This provides the softkeys on the left and right of the display, and allows you to set up the display functions.

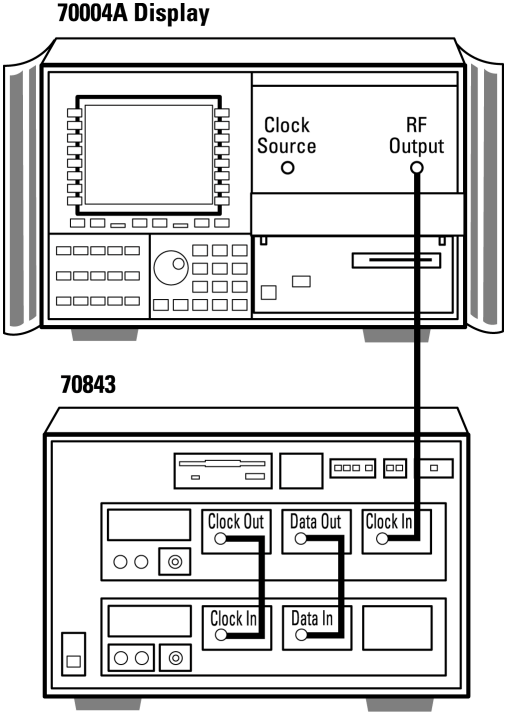
Access primary instrument functions by pressing MENU.

Both methods enable menus of softkeys that give access to all instrument functions.

Parameter Control Keys

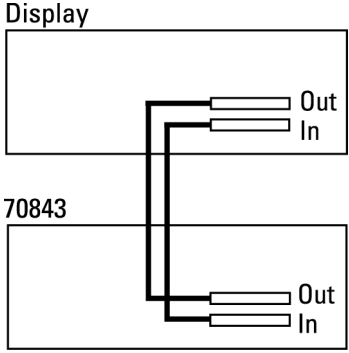
Display knob	Use the display RPG knob to change parameters and select operating values.
Numeric keypad	Use the numeric keypad to enter numeric values.
▲ ▼	Use the two step keys to change parameters up or down.

Front and Rear Panel Cabling



Front/Rear Cabling

System Back-to-Back Connection



HP-MSIB Cabling, rear panel

Front/Rear Cabling

Initial Switch-on

1. For a back-to-back system check, connect up the front panel as shown on page 9. Otherwise, connect up as appropriate to your application.
2. Connect the 70843 and 70004A rear-panel HP-MSIB ports as shown on page 10. If not, the red ***HP-MSIB*** LED on the display will light up.
3. Switch on the instruments in your system and check that all LEDs light up then go off after a few seconds. The green ***ACT*** LED on the 70843 will be lit up when the instrument owns the keyboard and display.
4. A lit up red ***E*** at the top left of the screen indicates an error in any instrument on row 0 of the address map. Refer to the 70004A Display ***Operation Manual*** for information about the address map. The red ***E*** also blinks if the display detects a fault on the HP-MSIB at power-up.

Pattern Generator Setup

Set Up Clock Output

Select [clock output] and setup the clock source frequency using the **SIG GEN FREQ**, **FREQ STEP**, **SIG GEN AMPLTD** and **SIG GEN ON OFF** softkeys.

Setup the internal clock parameters using the available softkeys.

The CLOCK and $\overline{\text{CLOCK}}$ OUT ports can be set to be independent, **C/TRCK ON OFF**, or track together, **C/TRCK ON OFF**.

Set Up Data Output

Select [data output] and use the softkeys displayed to select data output parameters.

The DATA and $\overline{\text{DATA}}$ OUT ports can be set to be independent, **D/TRCK ON OFF**, or track together, **D/TRCK ON OFF**.

Set Up Subrate Outputs

Select [subrate outputs] then use the available softkeys to setup clock/data parameters.

Pat Gen Setup

Add Errors

Select [error add] then either **ERR-ADD SINGLE**, **ERR-ADD EXTRNAL**, **ERR-ADD FIXED**, or **ERR-ADD OFF**.

Select Pattern Generator Trigger Output Pulse

The TRIGGER OUTPUT port gives an electrical trigger for use with an oscilloscope or other test equipment. Pattern or clock triggers are provided.

Clock trigger is a square wave at 1/8 or 1/32 of clock rate.

Pattern trigger is synchronized to repetitions of the output pattern. **For a pure PRBS**, it is one pulse per 32 repetitions; **for alternate patterns**, the trigger alternates with the pattern; and **for all other patterns**, the trigger pulse occurs at lowest common multiple of 256 and pattern length.

Pat Gen Setup

Select a pattern trigger as follows:

- **For a pure PRBS:** select trigger & setup, **PG TRIG PAT CLK**, **PG TRIG PATTERN** - enter ***PRBS code word*** using numeric keypad.
- **For alternate patterns:** select **PG TRIG A-B PAT**. Trigger pulse is at bit 0 of pattern or alternates with pattern A-B changeover.
- **For all other patterns:** select trigger & setup, then select ***pattern bit number*** using **PG TRIG BIT** and display RPG knob or numeric keypad.

Error Detector Setup

Set Up Data Input

Ensure the Error Detector is cabled correctly.

Select **input & eye** then setup input polarity, termination and delay using the available softkeys.

Perform clock-data alignment to ensure the Error Detector samples in the middle of the date eye as follows:

Select **input & eye**, **0/1 THR AUTOMAN**, **EYE EDG THRSHLD**, **CLK-DAT ALIGN**, **result pages**, **EYE RESULTS**, then view results.

On input signals with an unequal mark-density, perform a 0/1 threshold center operation as follows:

Select **input & eye**, **0/1 THR AUTOMAN**, **EYE EDG THRSHLD**, select eye edge threshold ratio using numeric keypad, then **CLK-DAT ALIGN**, **0/1 THR CENTER**, then view results.

Control Synchronization and Audible Tone

Select **sync & audio** and use the softkeys to control Error Detector synchronization and the audible tone that sounds when errors occur.

Synchronization to the incoming pattern can be performed automatically or manually. In manual, **START SYNC** forces the Error Detector to attempt synchronization with the received pattern. Synchronization is gained when the measured error rate is less than the set sync threshold.

Note that the sync softkeys are disabled (greyed out) when BURST GATING (on gating menu) is selected.

Errors Output Port

Produces a pulse that is the logical OR of errors in a 32-bit segment of data. Pulse length switchable - RZ or stretched (200 ns).

Select **trigger & setup**, **ERR O/P RZ 200ns**.

Select Error Detector Trigger Output Pulse

Select **trigger & setup** then set **ED TRIG PAT CLK** softkey to **PAT** or **CLK**.

Provides pattern and clock trigger.

Error Det Setup

Clock Trigger: a square wave at 1/8 of clock rate.

Pattern Trigger: for a pure PRBS, it is 1 pulse per 32 pattern repetitions. For all other patterns, pulse occurs at lowest common multiple of 256 and pattern length.

Measurement Gating

Start or Stop Gating

Start or stop gating at any time using **RUN GATING** and **STOP GATING**.

If your Display does not have a hardkey panel, select **MENU**, **gating** and use the **RUN GATING** and **STOP GATING**.

Note the green ***Gate*** flag at top right of the display during the measurement period.

Select a Measurement Period

Select **gating** then **MANUAL**, **SINGLE** or **REPEAT**.

Gate by Time, Bits or Errors

Select **SINGLE** or **REPEAT**; then **GATE BY TIME**, **GATE BY ERRS** or **GATE BY BITS**, then **GATING PERIOD**.

Meas Gating

If you select **GATE BY TIME**, use the numeric keypad then softkeys to select gating period.

Measurements

Basic BER Measurement

Press [RUN GATING] to start measurement.

Press [STOP GATING] to end measurement; view results on display.

Data Eye Measurement

Select [input & eye], **0/1 THR AUTOMAN**, **EYE EDG THRSHLD**, **CLK-DAT ALIGN**, [result pages], **EYE RESULTS**.

On input signals with an unequal mark-density, perform a 0/1 threshold center operation. Select [input & eye], **0/1 THR AUTOMAN**, **EYE EDG THRSHLD**, then select BER using numeric keypad, then **CLK-DAT ALIGN**, **0/1 THR CENTER**, [result pages], **EYE RESULTS**.

Measure-ments

Error Location Measurement

Define a specific bit in a ram-based pattern and perform measurements at that location. The bit specified is known as the BER location. There are three measurements: Bit BER, Block BER and Error Location Capture.

Bit BER

Select [error location], **BIT ERR ADDRESS** - use numeric keypad or display knob to select BIT ERR ADDRESS. Press [RUN GATING], at end of measurement period select [result pages], **OTHER RESULTS** to view Bit BER results.

Block BER

Select [error location], **BLOCK BER**, **BLOCK START** - use display knob or numeric keypad to select BLOCK START address, select **BLOCK LENGTH**, enter block length (must be a multiple of 32). Press [RUN GATING], [result pages], view results on **MAIN RESULTS** page at end of measurement period.

Error Location Capture

Select [error location], **CAPTURE ERROR**, view the error location in the Error Location Config window. Note, the **CAPTURE ERROR** softkey is greyed out if BLOCK BER is currently selected.

Measure-ments

Pattern Editor Operation

Select a Pattern

Select **pattern** then choose from one of five fixed pure **prbs** patterns, or a ram-based **zero sub**, **mark density** or **user pattern**.

Edit User Patterns

Select **pattern**, **edit ram user** or **edit disk user**, **INTERNL PATT** or **DISK PATT**. Select **toggle screen** for full screen. Use the softkeys displayed to edit the pattern.

Save a Pattern

Select **save pattern** then choose an **INTERNL PATT** or **DISK PATT** store.

Load a Block of Data

The block is loaded at the cursor point and tailored to fit between cursor and pattern end. **INSERT/REPLACE** determines whether bits are inserted or replaced.

Pat Editor Operation

Select **pattern**, **edit ram user** or **edit disk user**, **INTERNL PATT** or **DISK PATT** - set screen cursor to bit position where data block is to be loaded.

Set **INSERT/REPLACE** mode; **load block** - select a **prbs** or **user pattern**.

Save a Block of Data

Define a block of data within the current editor user pattern memory, then save the block to any pattern store large enough to hold the pattern. The current pattern store contents are overwritten by the new data being saved.

Select **pattern**, **edit ram user** or **edit disk user**, **INTERNL PATT** or **DISK PATT** - set cursor on first bit of block to be saved - select **savedel block** - set cursor on last bit of block (block shown underlined) - select **save to ram** or **save to disk**, **INTERNL PATT** or **DISK PATT** store.

Generate an Alternate Pattern

Select **pattern**, **edit ram user** or **edit disk user**, **CURRENT PATT**, **ALTPAT ON**, **YES**, **SET PAT LENGTH**, use numeric keypad, then press **ENTER**. You can load a prbs or user pattern into each half of the alternate pattern (use load block function).

Control Alternate Pattern Switching

You can control alternate patterns from the front panel AUXILIARY INPUT port or over HP-IB.

Select **pattern** - select an alternate pattern **ram user pattern** or **disk user pattern**, set **ALT PAT AUX USR** to **AUX** for control via the AUXILIARY INPUT, and **USR** for front panel control.

Disk Operation

Format a New Disk

Select `pattern`, `disk utils`, `format disk`, `FORMAT YES`.

Delete a Disk Pattern Store

Select `pattern`, `disk utils`, `delete diskpat`, then select the `DISK PATT` store to be deleted.

Disk Operation

General Functions

Set Keyboard Lock

Set Error Detector Real Time Clock

Update Firmware

Perform Self Test

For all of the above, select MENU, misc and select the appropriate softkeys.

Save/Recall Instrument setups

Select trigger & setup then recall setup or save setup.

Build Your Own Display of Results/Status Items

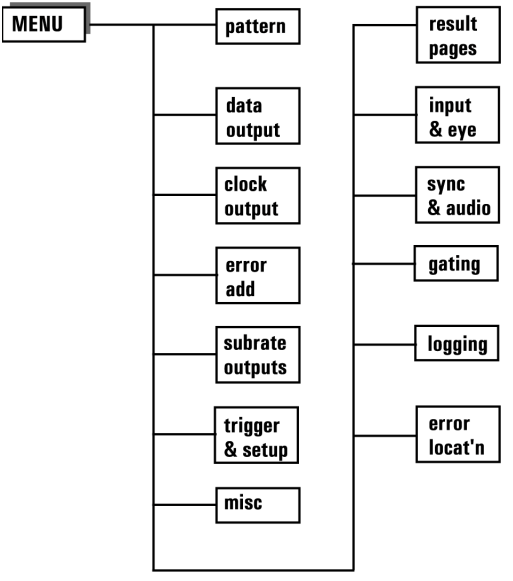
Select result pages, USER'S PAGE, build usr-pge - use the softkeys displayed to add/delete items from the user's page. Press CLEAR USR-PGE to delete all items from the user's page.

The Menus

The display instrument hardkey panel (when fitted) and the softkeys displayed when the MENU key is selected are used to select all major instrument functions. The following menu maps illustrate the softkey choices for each function or group of functions.

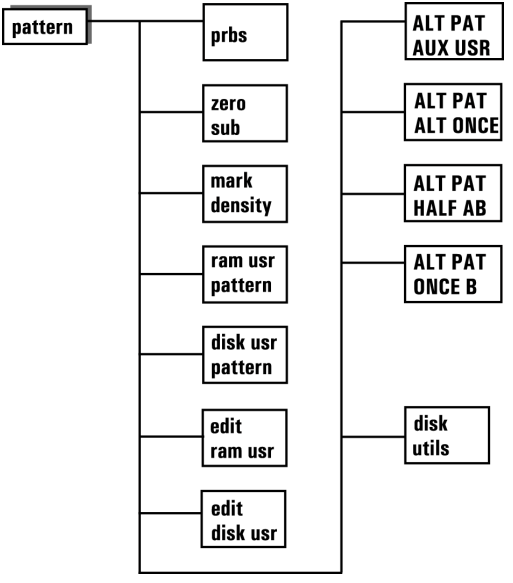
The boxes shown on the charts represent actual key presses and illustrate the sequence of key presses required to perform individual functions.

Main Menu



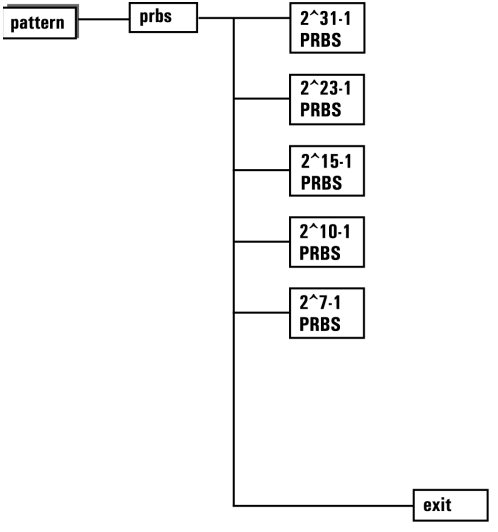
Notes:

Pattern



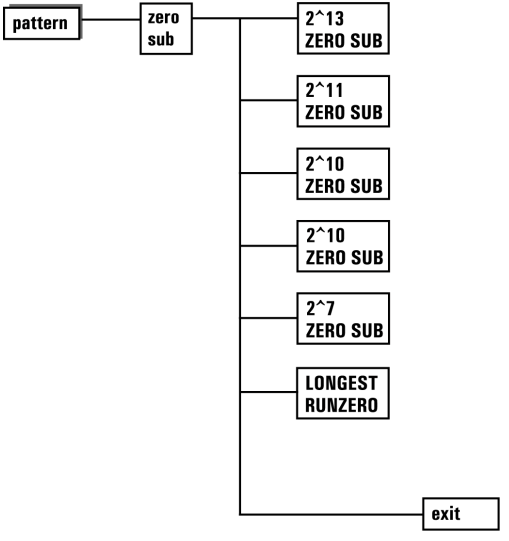
Notes:

Pattern - PRBS



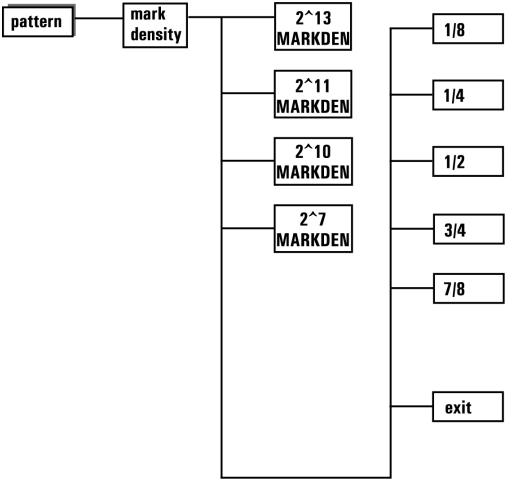
Notes:

Pattern - Zerosub



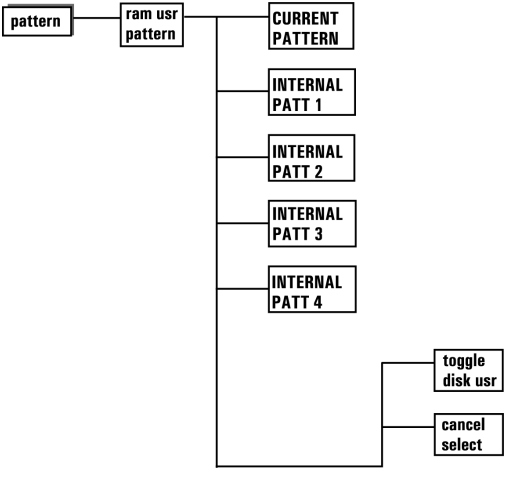
Notes:

Pattern - Markdensity



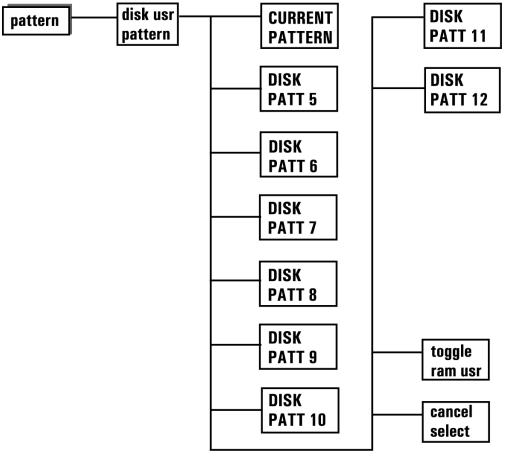
Notes:

Pattern - Ram User



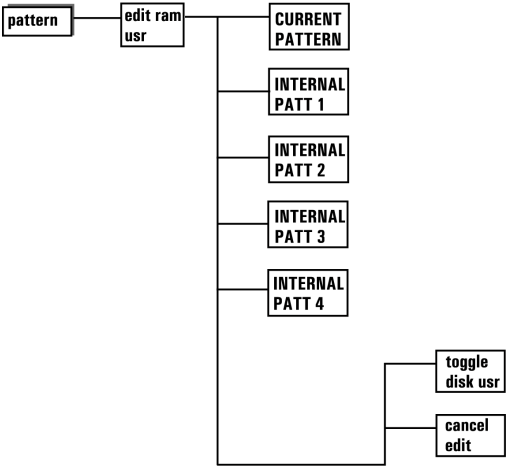
Notes:

Pattern - Disk User Pattern



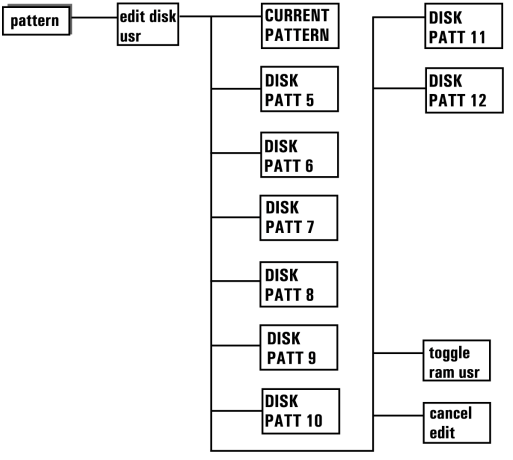
Notes:

Pattern - Edit Ram User



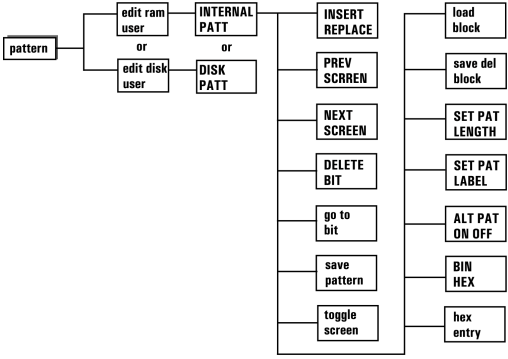
Notes:

Pattern - Edit Disk User



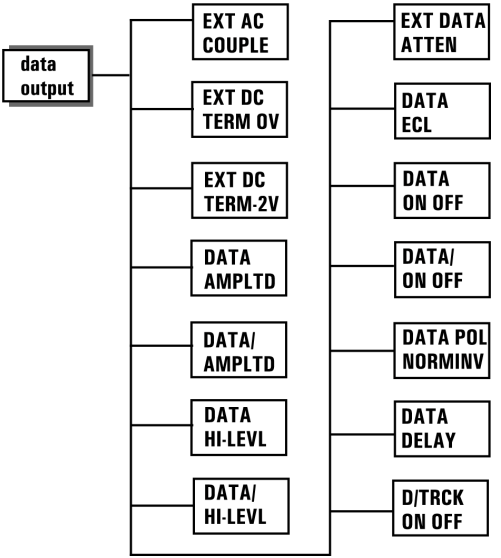
Notes:

Pattern - Edit User



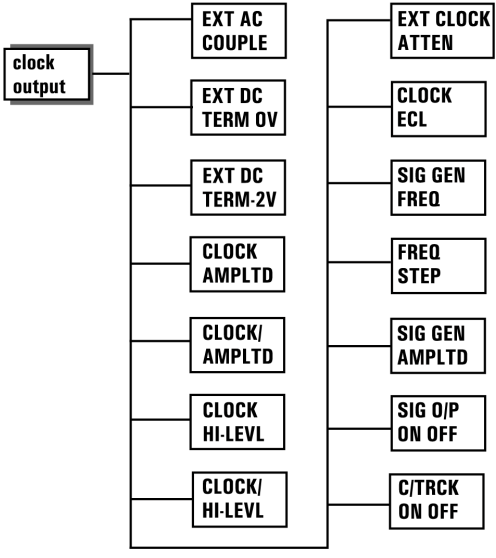
Notes:

Data Output



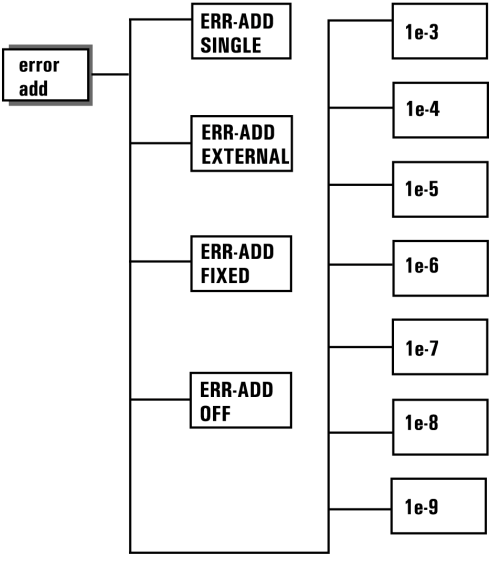
Notes:

Clock Output



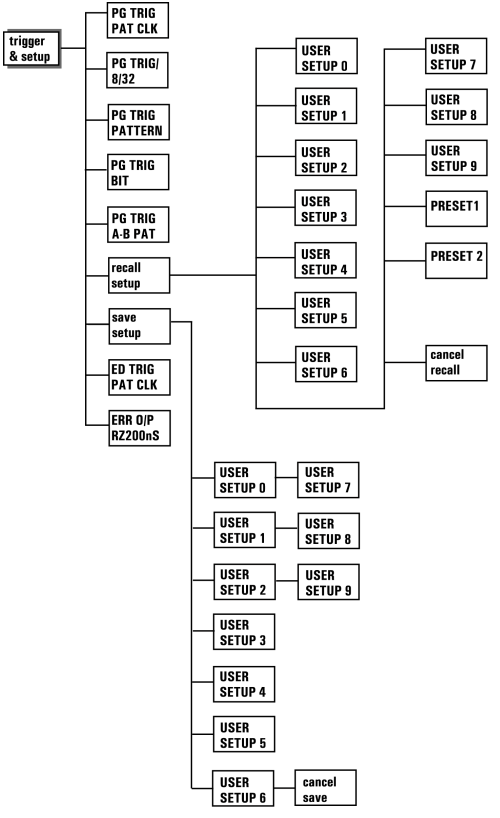
Notes:

Error Add

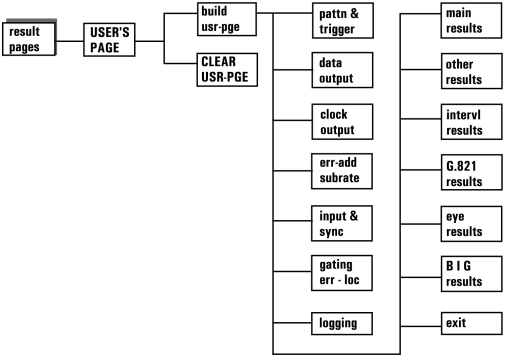


Notes:

Trigger & Setup



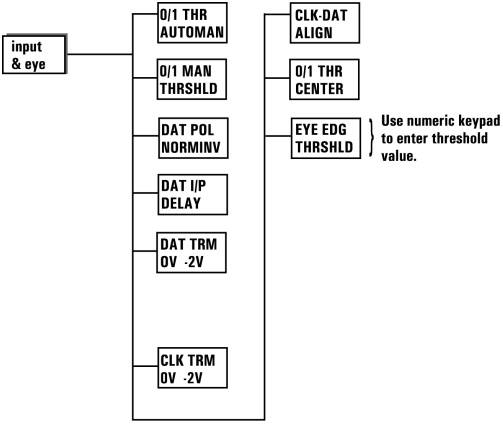
Result Pages



The Menus

Notes:

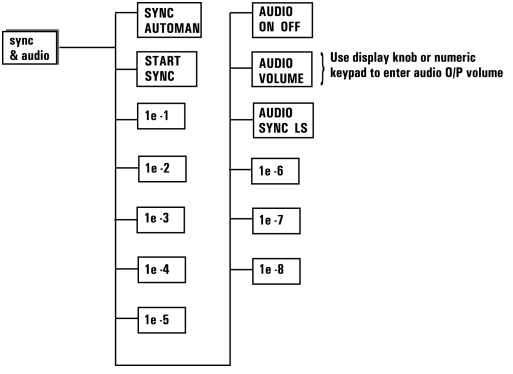
Input & Eye



Notes:

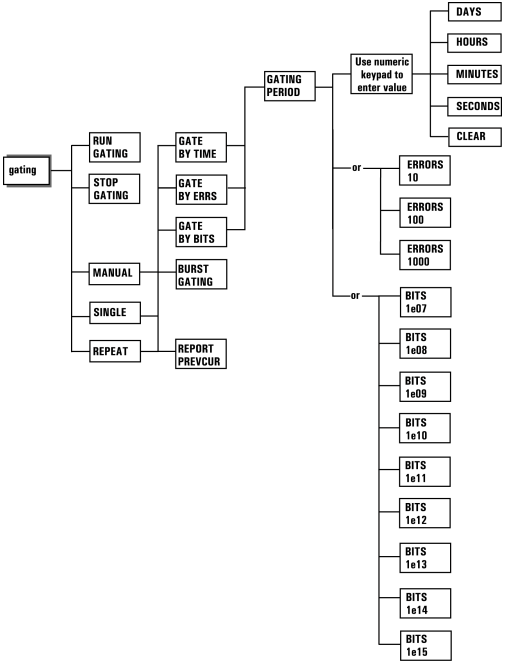
The Menus

Sync & Audio



Notes:

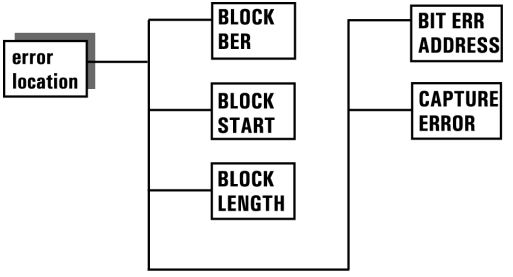
Gating



Notes:

The Menus

Error Location



Notes:

BER Basics

Bit Error Ratio (BER) is the most fundamental measure of system performance - how well bits are transferred end-to-end. While this performance is affected by factors such as signal-to-noise and distortion, ultimately it is the ability to receive information error-free that defines the quality of the link.

$$\text{BER} = \frac{\text{Number of bits received in error}}{\text{Number of bits received}}$$

$$= \frac{\text{Error count in measurement period}}{\text{(Bit rate) x (measurement period)}}$$

A Bit Error Ratio Tester (BERT) measures BER on systems and components. Usually BERTs are made of two components, the Pattern Generator (PG) and the Error Detector (ED). They can provide test data sequences, and also measure error ratio. Often the two components are used together, but not always - a PG makes an ideal stimulus for component design work. In some BERTs, the clock source may also be separate.

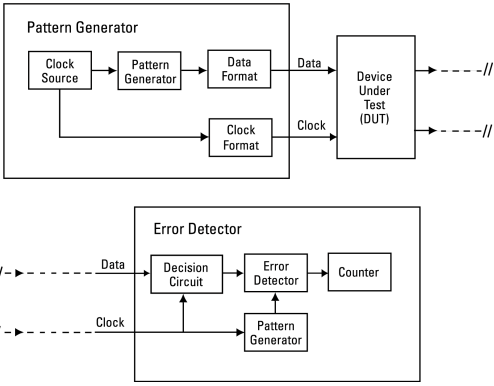
A BERT makes physical layer measurements and differs from a protocol or SONET tester in the following ways. A BERT can usually:

- Vary voltage levels.
- Vary the timing relationship between clock and data.
- Vary the clock frequency significantly.

See over the page for a block diagram showing a Pattern Generator and Error Detector.

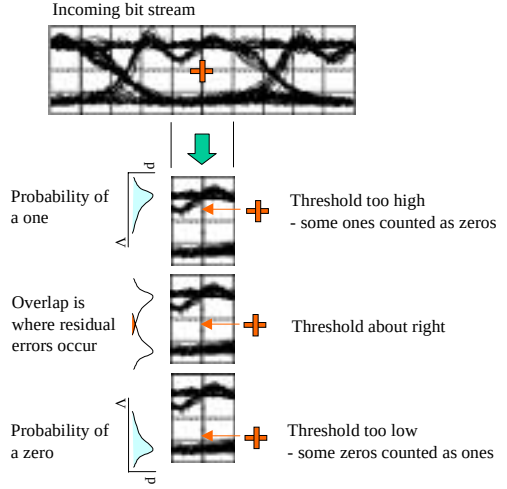
BER - What is it?

BER -
What is it?



BERT Decision Threshold

The decision threshold is the point above which voltages are counted as a one, and below which it is counted as a zero. This decision is made on every incoming bit, turning an analog value into a digital stream of ones and zeros. For both test instruments and network equipment, the key to accurately representing the incoming signal is in getting the position of this decision point correct. This means getting both the (vertical) decision threshold voltage and the (horizontal) clock-data delay correctly set. The clock-data delay must be adjusted so that the decision point is positioned at the center of the bit period.

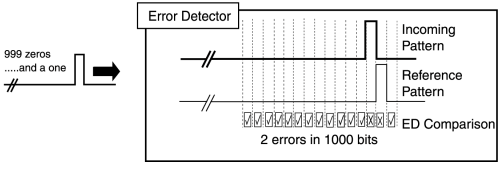


BER - What is it?

False Sync

False sync occurs when the equipment tries to achieve synchronization, and although the error ratio falls below the sync threshold value set, it is not properly synchronized. This can happen with certain user-based patterns but not with a PRBS.

For example:
Imagine a pattern with 999 zeros followed by a single one. As the error detector tries to achieve synchronization, most comparisons of incoming pattern to reference pattern yield an error ratio of $2x10^{-3}$. Only one position gives error free operation. However, the error ratio in the other positions could easily be better than the synchronization threshold set, and thus the error detector will say it has achieved satisfactory operation.



Look for this when there is a stable error ratio which cannot be explained in any other way. Change the sync threshold value to a lower one - for example, from 10^{-1} to 10^{-7}. Synchronization will not be as fast with a more stringent threshold but will be more accurate.

Test Time, Confidence Interval and Residual BER

BER is a statistical measure. It is not possible to predict with certainty when errors will occur. Therefore, how do you know when you have tested error-free for long enough to say that you really have better than 10^{-14} BER performance?

When testing systems it is important to test at the full line rate to minimize the test time, without compromising the measurement integrity (i.e. confidence in the results).

$$C = 1 - e^{-nb}$$

where C = degree of confidence (0.95 = 95% confidence)

n = number of bits examined with no error detected

b = desired residual BER

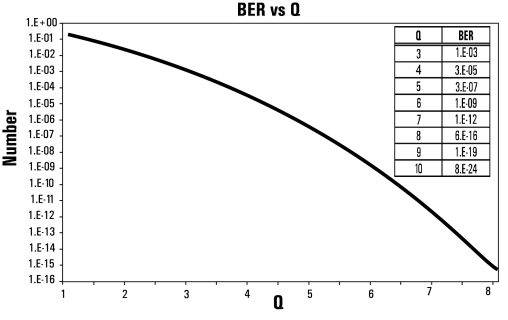
BER	Approx Test Time for 95% Confidence Level				
	STM-256/ OC-768	STM-64/ OC-192	STM-16c/ OC-48c	STM-4c/ OC-12c	STM-1/ OC-3
$1x10^{-20}$	240 year	960 year	3.8k year	15.2k year	61k year
$1x10^{-16}$	8.7 day	35 day	139 day	1.5 year	6.1 year
$1x10^{-15}$	21 hr	3.5 day	14 day	56 day	224 day
$1x10^{-14}$	2.1 hr	8.4 hr	1.4 day	5.6 day	22.4 day
$1x10^{-13}$	12.5 min	50 min	3.3 hr	13 hr	2.2 day
$1x10^{-12}$	1.3 min	5 min	20 min	80 min	5.3 hr
$1x10^{-11}$	7.5 sec	30 sec	2 min	8 min	32 min
$1x10^{-10}$	1 sec	3 sec	12 sec	48 sec	3.2 min

BER - What is it?

Q Factor

BER - What is it?

Q is a measure of the electrical signal-to-noise ratio of the system at the receiver decision threshold. BER may be estimated from Q when it is impractical to measure using conventional techniques. Q factor is a figure of merit often used in optically amplified systems in which noise from the amplifiers dominates receiver noise.



Q factor is usually measured using either network equipment receiver electronics or a BERT, in each case using the ability to vary the decision threshold. The BER is recorded versus decision level down the centre of the eye.

As the decision threshold is moved towards the "1" and "0" levels the BER becomes dominated by the noise on those levels. The data may be divided into two sets dominated by error ones and zeros.

The data is separated at the point of minimum error rate for measurable BER's and each set is fitted to an ideal curve assuming Gaussian noise statistics.

The equivalent mean and standard deviation are derived from the slope and intercept of the fitted curve.

Q factor can also be measured using a digitizing oscilloscope, although this is less accurate; oscilloscopes do not sample every bit transmitted, and the measurement can become dominated by the front-end electronics of the instrument rather than the system under test.

- Q is defined as:

$$Q = \frac{I_1 - I_0}{\delta_1 + \delta_0}$$

where

I_1 = mean level of a “1”
I_0 = mean level of a “0”
δ_1 = standard deviation of a “1”
δ_0 = standard deviation of a “0”

$$BER = \frac{1}{2} erfc\frac{(Q)}{\sqrt{2}} \approx \frac{\exp(-Q^2/2)}{Q\sqrt{2\pi}}$$

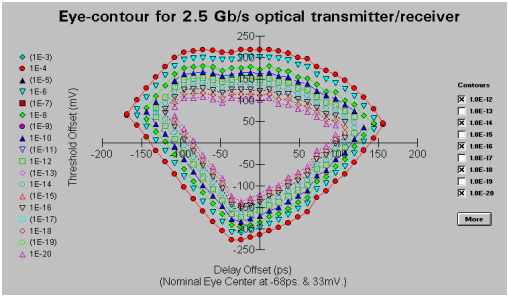
Approximate form of BER expression is reasonably accurate for Q>3 and is therefore appropriate for all practical BERs.

BER - What is it?

Eye Contour Measurements

BER - What is it?

Eye contours plot the inside of the eye as a function of BER. They enable a quantitative understanding of the eye diagram and can show degradations such as noise and inter-symbol interference when used with appropriate test patterns. They also allow observation of low-probability impairments and a visible indication of sampling point margin.

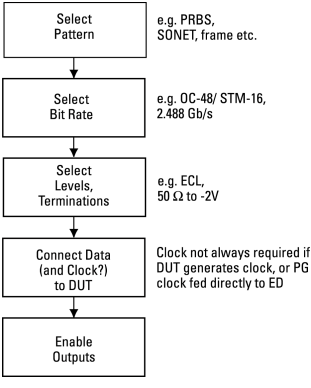


(Plot produced by E4543A application software)

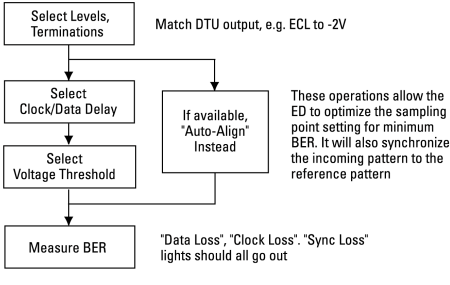
BERT Troubleshooting

Setting up a Simple BER Measurement

Pattern Generator setup



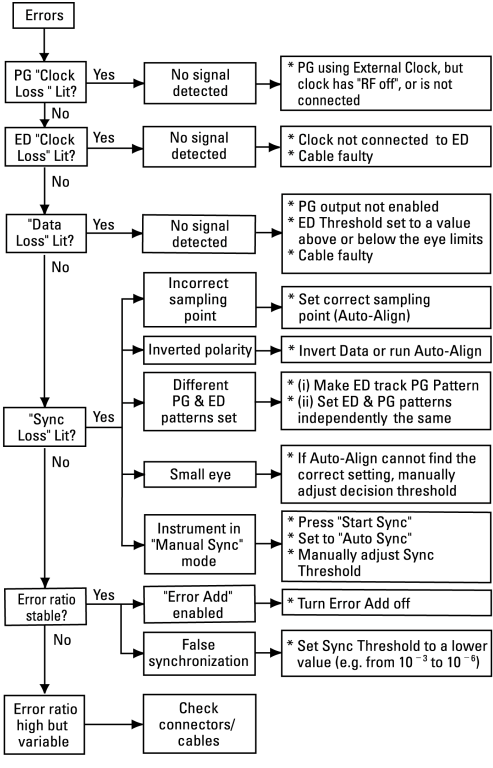
Error Detector setup



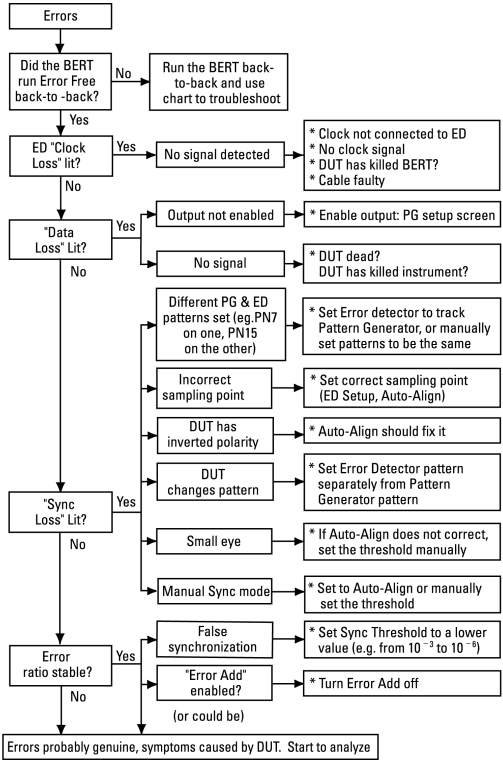
BER - What is it?

BERT Connected Back-to-Back

BER - What is it?



BERT Connected to DUT



BER - What is it?

Properties of PRBSs

BER - What is it?

Why use PRBSs?

- They simulate random data.
- The data sequence is deterministic. The pattern repeats and can be predicted to infinity.
- Easy to generate and measure them at high speed.
- Easy to vary the ones (mark) density. Many systems are ac coupled so this becomes an easy way of putting the pattern out of balance in a randomly distributed way. Helps to check for base-line wander, and so on.
- Not harmonically related to the data rate. Simulates all possible combinations of the data.
- Spectral content allows use as a noise source.
- Decimation.
- Allows results to be compared against theory.

PRBSs

Pseudo Random Bit (or Binary) Sequences are an accepted way of testing digital circuits in many industries from radar, tape drives and hard disks to satellite communication and fiber optics. In all of these, the quality of a system is based on its ability to pass data error-free. PRBSs provide a means to simulate the type of traffic that the system is likely to see. They also provide a means to stress that system to its limits.

For example:

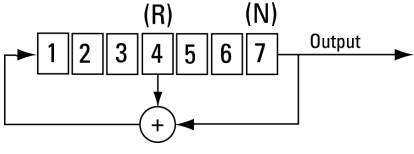
- Long strings of ones or zeros will show low frequency circuit defects
- Clock recovery circuits find long runs of ones or zeros hard to deal with and may lose lock.

- Gallium Arsenide circuits can suffer from “slow tail” - long runs of zeros or ones allow capacitive charging of the circuit which can cause the first one or zero that comes afterwards to fail to attain a full logic level voltage.
- An isolated one amongst a string of zeros will tend to show high frequency circuit defects

PRBS Generation

PRBSs are usually generated by a series of ‘N’ shift registers connected together. The output, and one or more other points are XOR’ed together and fed back to the input. Any random seed will go to a known state, unless all zeros are present - this will stay as all zeros forever. The tap point, ‘R’, is standardized for common sequences.

The commonly used PRBSs have combinations of ‘R’ and ‘N’ that cause them to be “maximal length” - not all combinations cause the resulting streams to contain all possible word sequences unless they are maximal length.



BER - What is it?

Properties of PRBSs

BER - What is it?

- Balanced - the number of ones equals the number of zeros within ±1.
- Compare sequence with itself - get 50% error ratio in all positions except exact correlation where it is error free.
- '0000…' condition never appears as it would lock up the shift registers - hence "2^n-1".
- 2^n-1 will contain a maximum run of "n" ones, "n-1" zeros. Does not repeat for maximal length sequences.

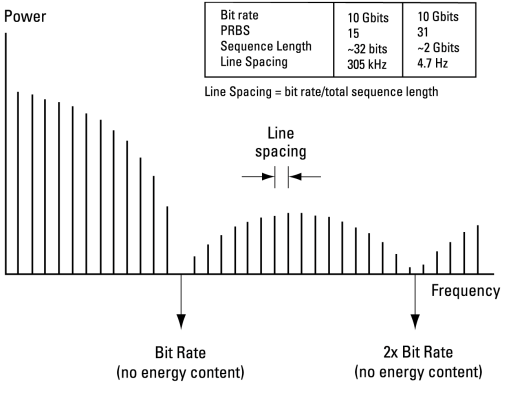
'n'	Sequence length (bits)	Longest run of ones	Longest run of zeros
7*	127	7	6
10	1023	10	9
11	2047	11	10
15*	32,767	15	14
20	1,048,575	20	19
23*	8,388,607	23	22
31	2,147,483,647	31	30

* ITU Standard

PRBS Frequency Spectrum

Digital NRZ data has a sin x/x characteristic spectrum. PRBS follows this envelope, with line spectra of a spacing related to the sequence repetition rate. The longer the sequence before it repeats, the narrower the line spacing.

The closer to a continuous spectrum produced, the more like an analog noise source the test signal looks. The benefit of this is that such a stimulus will show up any frequency dependent effects in a device under test. For example, a clock recovery circuit designed to lock onto a single frequency may have a tendency to lock onto harmonics. A long PRBS may uncover such undesirable behavior.

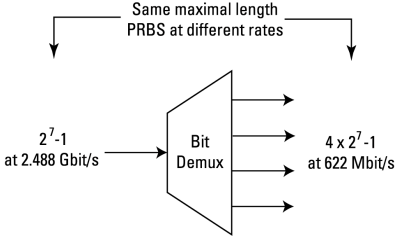


BER - What is it?

Decimation

BER - What is it?

Demultiplex a PRBS through a demux with 2^n ports (2, 4, 8, 16, and so on) and the output of each will be the same PRBS sequence at lower speed with different phases. The same is true for multiplexing - most test equipment will generate multiple streams of PRBS at low speed and combine them at the end into one high speed stream.



With decimation of a PRBS, if every 2^n bits of a PRBS is selected, the result is the same PRBS data but each sequence is phase-shifted by $(2^n-1)/2^n$ bits from the others (that is, sequence length/decimation factor). For example, decimate a 2^4-1 sequence by 2:

Original 2^4-1: **0**1011001000111**0**10110010001111

Odd bits: **0 0 1 0 0 0 1 1 1 1 0 1 0 1 1**

Even bits: **1 1 0 1 0 1 1 0 0 1 0 0 0 1 1**

Sequence length/decimation factor = 15/2 = 7.5 (8 bits).

(Note: **0** indicates the start of the sequence.)

Logic Levels, Terminations and Data Rates

Logic Levels

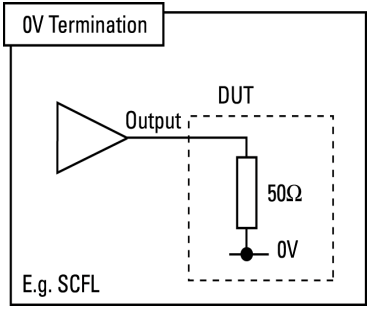
Family	SCFL	ECL	PECL
V_{hi}	0 V	-0.9 V	4.1 V
V_{lo}	-0.9 V	-1.75 V	3.25 V
V_{pp}	900 mV	850 mV	850 mV
Termination	0 V	-2 V	+3 V
Z	50 Ω	50 Ω	50 Ω
Supply	0/-3.5 V	0/-5.2 V	5/0 V

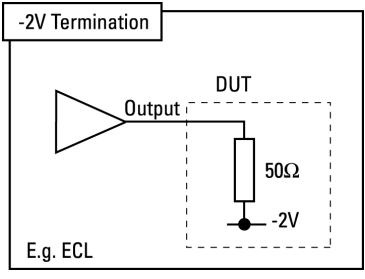
Family	LVPECL	TTL	LVTTL
V_{hi}	2.4 V	>2.4 V	>2.0 V
V_{lo}	1.55 V	<0.8 V	<0.8 V
V_{pp}	850 mV		
Termination	+1.3 V		
Z	50 Ω		
Supply	3.3/0 V	5/0 V	3.3/0 V

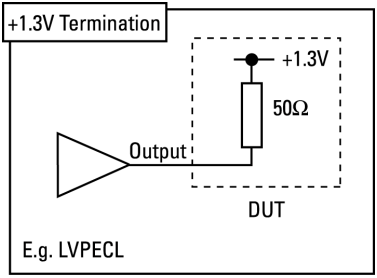
BER - What is it?

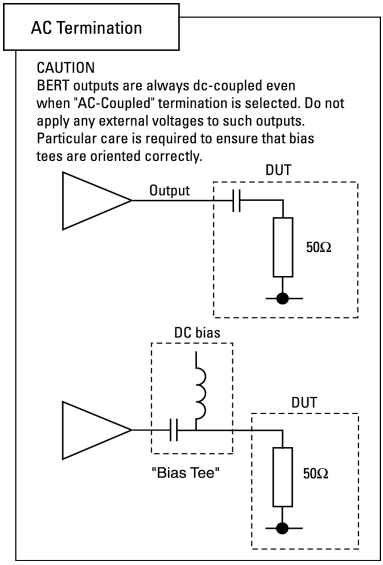
Terminations

BER -
What is it?









BER - What is it?

Common Data Rates

BER - What is it?

Selected Telecom Rates		
North American	**European**	**Rate**
DS 1		1.54 Mb/s
DS 3		44.736 Mb/s
	E1	2.048 Mb/s
	E3	34.368 Mb/s
	E4	139.264 Mb/s
OC-1	STM-0	51.84 Mb/s
OC-3	STM-1	155.520 Mb/s
OC-12	STM-4	622.08 Mb/s
OC-48	STM-16	2.48832 Gb/s
OC-192	STM-64	9.95328 Gb/s
OC-768	STM-256	39.81312 Gb/s

Selected Enterprise Rates	
Name	**Rate**
Ethernet (with coding)	12.5 Mb/s
Fast Ethernet	125 Mb/s
Gigabit Ethernet	1.25 Gb/s
2 x Gigabit Ethernet	2.5 Gb/s
10 x Gigabit Ethernet	9.95 Gb/s
or	12.5 Gb/s
or 4 channels at	3.125 Gb/s
Fiber Channel	1.063 Gb/s
2 x Fiber Channel	2.12 Gb/s